Delta Modulation Codec for Telephone Transmission and Switching Applications

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A highly integrable delta modulation codec design, for applications where transmission bandwidth is not at a premium but where an inexpensive and high quality converter is desired, is considered in this paper. An asymmetrical codec integrator is used to improve quantizing noise characteristics. Charge parceling techniques which are used for performing the integrating function, offer advantage over conventional RC integrators.

I. INTRODUCTION

Delta modulation[1] (ΔM) is receiving interest for voiceband analog-to-digital (A/D) conversion applications where coding efficiency is less important than the requirement for economical, but high quality A/D conversion, characteristics. One of the potential applications is in pulse code modulation (PCM) coding systems where the PCM code is formed by first converting the analog signals into a single bit digital code using per terminal ΔM coders. The ΔM bit stream is then converted into a PCM format using digital filtering.[2,3] The technique takes advantage of the simple means of providing A/D conversion with ΔM and utilizes highly integrable digital hardware for providing the ΔM to PCM conversion.

Another promising application of ΔM is in space division switching networks. Analog inputs to the network are converted into a digital code by per terminal ΔM coders. This allows implementation of digital switching networks which are more ideally suited to integrated semiconductor technology than analog networks. Requirements on network loss, signal distortion and crosstalk are significantly relieved.

We describe the design of a single integration ΔM codec (*co*der-*dec*oder) which shows promise of meeting the conversion requirements for both of the above applications. Improved conversion characteristics

are achieved using planned integrator asymmetry. For accurate coding characteristics at high clock (sampling) rates, charge parceling techniques are used in the integrator for reconstructing the analog signals. A highly integrable design which offers economical, per line A/D conversion is achieved.

II. DELTA MODULATION CODING REQUIREMENTS

2.1 *Codec Operation*

A block diagram of a delta modulation codec, using single integration, is shown in Fig. 1. To perform the analog-to-digital conversion, an analog input is compared with a reconstructed version of itself from the coder integrator. The relative difference between the signals is translated into a single bit digital code by clocking the output of the comparator stage. The code is then transmitted to both coder and decoder integrators where it forces either a small positive or negative voltage change in the integrator output. Thus, a single bit code is used for controlling the integrator voltage and causes the integrator to produce a close track of the input signal. If a matched integrator is placed at the decoder, a similar track of the analog signal is recovered.

2.2 *Overload Characteristics*

Because the transmitted digital code contains information corresponding to the derivative of the message function, overload characteristics with delta modulation become a function of signal slope instead of amplitude. The overload point occurs when the integrator is forced to produce a similar polarity voltage step during each clock cycle. Thus,

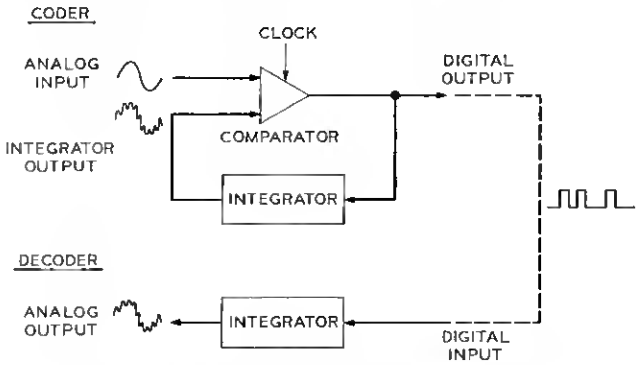

Fig. 1—Delta modulation codec (*co*der-*dec*oder).

for a sampling frequency, f_s, and an integrator step, σ, the maximum integrator voltage slope is given by

$$\sigma f_s .$$

The maximum slope of a sine wave of amplitude, A, and frequency, f, is

$$2\pi f A,$$

and therefore overload occurs when

$$2\pi f A \geqq \sigma f_s . \tag{1}$$

This sets the product of σ and f_s; their relative values are set by quantizing noise requirements for meeting signal to noise objectives.

2.3 *Quantizing Noise*

Granular quantizing noise has been the subject of numerous papers including works by Van de Weg,[4] Wang,[5] and Iwersen.[6] The theory developed by Iwersen predicts a quantizing noise spectrum which is in good agreement with measured noise in delta modulators.[7] To improve noise characteristics of our delta modulator, his theory is used for optimizing coding characteristics. Some of the basic equations and calculations which govern the design of our codec are reviewed in this section. A detailed description is given in Ref. 6.

The effect of an asymmetrical integrator is shown in Fig. 2, where coding of an idle channel input or a dc signal is illustrated. In this example, the positive integrator step, σ_+, is larger than the negative step, σ_-; that is,

$$\sigma_+ = \sigma + \epsilon,$$

$$\sigma_- = -\sigma + \epsilon.$$

As a result, a sawtooth error wave of peak-to-peak amplitude σ is generated. The noise spectrum resulting from coding a steady-state input with unbalanced integrators consists of frequencies given by

$$f_l = | Q[l(1 - \vartheta)/2]f_s | \tag{2}$$

where

$$Q(\alpha) = \alpha - N(\alpha).$$

$N(\alpha)$ is the integer nearest α, and

$$\vartheta = \epsilon/\sigma.$$

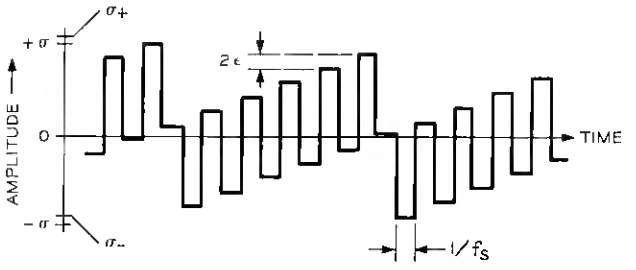

Fig. 2—Integrator output for an asymmetrical coder, shown with $|\sigma_+| > |\sigma_-|$.

The power at the frequency of index l is calculated from

$$P_l = 2\sigma^2/\pi^2 l^2. \tag{3}$$

The frequencies for which l is even are components of the sawtooth wave of peak-to-peak amplitude σ and fundamental frequency ϑf_s. Additional, not so evident, sawteeth are also usually present. For example, components of a second order sawtooth are calculated by choosing values of l equal to aN, where a is a positive integer and N is the odd integer nearest $1/\vartheta$. This sawtooth has a peak-to-peak amplitude of $2\sigma/N \approx 2\epsilon$ and a fundamental frequency of $|\,(1 - N\vartheta)f_s/2\,|$.

It is possible to significantly reduce inband quantizing noise for low level inputs by using a planned integrator imbalance.[8,9] However, to guarantee good noise characteristics, the imbalance must be maintained between a lower and an upper limit. The lower limit must allow an imbalance to force the fundamental component of the fundamental sawtooth wave above voiceband. The change (the spreading) of the noise spectral lines resulting from phase modulation of the idle channel spectrum by the input signal must also be considered.

The upper limit on integrator imbalance is set by quantizing noise objectives. It is difficult to guarantee that the fundamental component of the second order sawtooth wave (of peak-to-peak amplitude $\approx 2\epsilon$) will be kept out of voiceband. Therefore, the magnitude of the integrator step imbalance, ϵ, must be maintained at a level where it will not introduce excessive inband noise problems at low or quiescent input levels.

Iwersen has calculated the quantizing noise as a function of signal level for various step imbalances using a 12-millivolt integrator step size and a 1.544-MHz sampling rate. The calculation is made for a broadband input and uses C-message weigbting of the noise in the voiceband. Results are plotted in Fig. 3. The advantage of using an

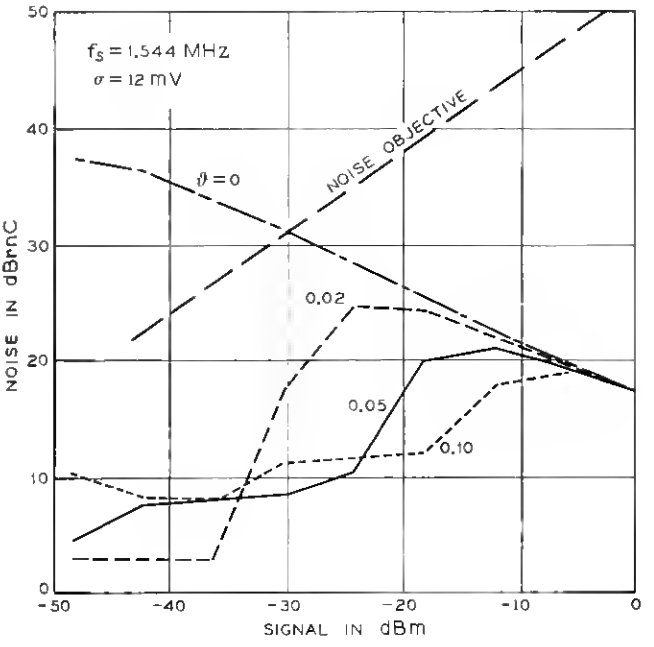

Fig. 3—Calculated quantizing noise versus average speech power for ϑ = 0, 0.02, 0.05, and 0.10.

asymmetrical integrator over a perfectly balanced integrator ($\vartheta = 0$) is clearly evident for low level input signals. An optimal range of integrator imbalance falls into a range from $\vartheta = .02$ to $\vartheta = 0.10$. At higher values of ϑ increased quantizing noise is produced at quiescent levels and at low signal levels. For lower values of ϑ, the fundamental sawtooth frequency is close to voiceband and phase modulation of the spectral lines due to input signals causes excessive quantizing noise energy to fall into voiceband.

2.4 *Transmission Objectives*

Design objectives for this experiment* require that coding a 6-volt peak-to-peak (+7 dBm into 900Ω), 1000-Hz signal will not cause slope overloading. This corresponds to a maximum integrator voltage slope

* The design objectives should not be interpreted as official Bell System transmission objectives. They were established for this experiment as a guide line for providing a reasonable quality of voiceband conversion.

capability of

$$\sigma f_s \approx 19 \times 10^3 \text{ volts/second.}$$

Additional design objectives include a 50-dB dynamic range with a signal-to-noise ratio better than 25 dB at the −43-dBm level, increasing to better than 40 dB at the +7-dBm level. Quantizing noise of idle channels (zero input) should he maintained helow 16 dBrn using C-message weighting. Design objectives for gain (loss) variation, over a 200-Hz to 3200-Hz frequency handwidth, require an average 0.5-dB loss with loss variation maintained within ±0.25 dB.

III. CODEC CIRCUIT DESIGN

The relative simplicity of the delta modulation coding function makes feasible the realization of highly integrable and inexpensive codec configurations. In this design, the codec circuitry utilizes a combination of integrated semiconductor and thin-film capacitor techniques and relies heavily on the characteristics of the two technologies—excellent matching of device characteristics on an integrated circuit (IC) chip and close ratio tolerances hetween capacitors on thin-film capacitor arrays. These characteristics are of special importance in the key elemcnt of the codec, thc intcgrator network, where a high degree of precision is needed for accurately rcconstructing an analog signal from a digital input signal.

3.1 *Charge Parceling*

The integrator utilizes a charge parceling circuit (sometimes called the "hucket and dipper" circuit), shown in Fig. 4, to provide the digital-to-analog conversion function. The prime advantage of the charge parceling approach is that it relies only on capacitor ratio tolerances for making the digital-to-analog conversion rather than on absolute resistor and capacitor tolerances required hy the more commonly used RC type integrators. Timing problems are also not critical, provided sufficient time is allowed for charging and discharging small charge parceling capacitors in the integrator network.

To add a voltage step to the integrating capacitor, C_I, (Fig. 4) the +1 input (clock input) is applied to produce a positive voltage step of ΔV at the C_{+1} capacitor terminal. This causes an equivalent change in voltage on both of the capacitor terminals until the increase exceeds the threshold of T_2. As T_2 turns on, charge is dumped from C_{+1} to C_I, producing a voltage step on C_I proportional to the two capacitors

$$\Delta V_I = \left[\frac{C_{+1}}{C_I + C_{+1}}\right]\Delta V' \tag{4}$$

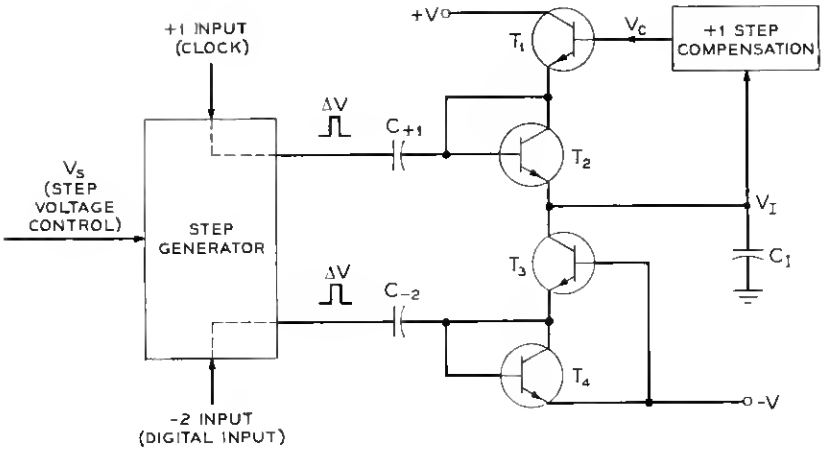

Fig. 4—Charge parceling circuit for ΔM integrator.

where ΔV_I is the voltage change on C_I and $\Delta V'$ is the voltage change at the C_{+1} terminal after T_2 begins to conduct.

As the input returns to its original level, a negative voltage step of ΔV is forced on the C_{+1} terminals. This change causes T_2 to become reverse biased and turns T_1 on to recharge the C_{+1} capacitor. The recharge voltage for C_{+1} is governed by the compensation network which translates a voltage V_c, approximately equal to the integrating capacitor voltage V_I, to the base of T_1. Thus, C_{+1} is recharged to V_c minus the base to emitter drop of T_1, and the net increase in integrator voltage due to a +1 input is

$$\sigma_{+1} = \Delta V_I = [\Delta V - V_{BE_{T_1}} - V_{BE_{T_2}} - (V_I - V_c)] \left(\frac{C_{+1}}{C_I + C_{+1}}\right). \tag{5}$$

Note that the effect of the junction capacitances of T_1 and T_2 also must be considered in the step size calculation, but the effect is secondary and is not described in detail here. Equations including junction capacitances are given in the appendix.

Changes due to temperature in the threshold voltages of $V_{BE_{T_1}}$ and $V_{BE_{T_2}}$ are compensated by controlling the amplitude of the voltage step (ΔV) with a dc voltage V_c and two matching base to emitter (diode) voltages V_D. Therefore, the effective +1 integrator step can be rep-

resented as

$$\sigma_{+1} = [V_s + 2V_D - 2V_{BE} - (V_I - V_c)]\left(\frac{C_{+1}}{C_I + C_{+1}}\right). \quad (6)$$

To produce a negative step to the integrator the -2 input (digital input) is activated. This causes a voltage change on C_{-2} similar to the change produced on C_{+1} by the $+1$ input. However, charge is removed from C_I during the negative slope of ΔV and is dumped from C_{-2} to the $-V$ supply during the positive slope of ΔV. The effective voltage step produced at the integrating capacitor by this input is given by

$$\sigma_{-2} = [V_s + 2V_D - 2V_{BE} - (V_I - V_c)]\left(\frac{\alpha_F C_{-2}}{C_I + \alpha_F C_{-2}}\right) \quad (7)$$

where α_F is the common base current gain of T_3. To minimize the effect of α_F variation, a Darlington transistor pair is planned as a replacement for T_3 in future models.

In the delta modulation codec, a clock controls the $+1$ step input to the integrator, and consequently a σ_{+1} step is added to the integrator during each clock cycle. The digital input to the integrator controls the -2 step input. When present, it decreases the integrator voltage by σ_{-2}. Therefore, whenever a digital input is applied, the net change in the integrator voltage is $\sigma_{+1} - \sigma_{-2}$. When the digital input is not applied, the clock automatically raises the integrator by a σ_{+1} step.

To optimize quantizing noise characteristics, the integrator asymmetry is designed for

$$0.02 < \vartheta < 0.10$$

or, translated to the integrator step requirements (for the case $\sigma_+ > \sigma_-$)

$$\frac{\sigma_{-2}}{\sigma_{+1}} = 1.89 \pm 0.07.$$

An additional feature of the charge parceling integrator is that gain (or loss) between coder and decoder integrators can be easily adjusted. Gain can be adjusted either by changing the step generator voltage, V_s, between integrators or by using a different ratio of integrating to charge parceling capacitors on the coder and decoder integrators. The first technique might be useful as a form of automatic gain control which can be adjusted as a function of voltage. The second technique would be useful when a predetermined amount of gain (or loss) is desired.

3.2 *Compensation Network*

To prevent the decoder output from drifting to either a maximum positive or negative output voltage as a result of differences in the plus

and minus steps between the coder and decoder integrators, the decoder integrator must compensate to automatically adjust its step imbalance to match the coder integrator step imbalance. Compensation is not needed in the coder integrator but is added to help match coding characteristics between coder and decoder.

With the charge parceling circuits described, compensation is achieved by adjusting σ_{+1} of the decoder integrator as a function of the integrator voltage level. The step size is varied by adjusting the recharge voltage for the C_{+1} capacitor.

Figure 5 shows a schematic of the compensation network. A nearly linear compensation as a function of integrator output voltage is achieved by this configuration. Good reproducibility of compensation characteristics between integrators is also possible. Operation is as follows.

With no current through R_2, a voltage equivalent to V_I is translated to the base of T_6 for recharging the $+1$ step capacitor, C_{+1}. As V_I increases above this level, V_C also increases but begins to lag farther and farther behind V_I, because R_1 can no longer supply all of the current required by the current source I_2. The balance of the current is supplied through R_2, and the voltage drop across R_2 determines the difference between V_C and V_I.

The opposite happens as the integrator voltage drops below the bias point set by R_1 and I_2. Then R_1 will supply more current than accept-

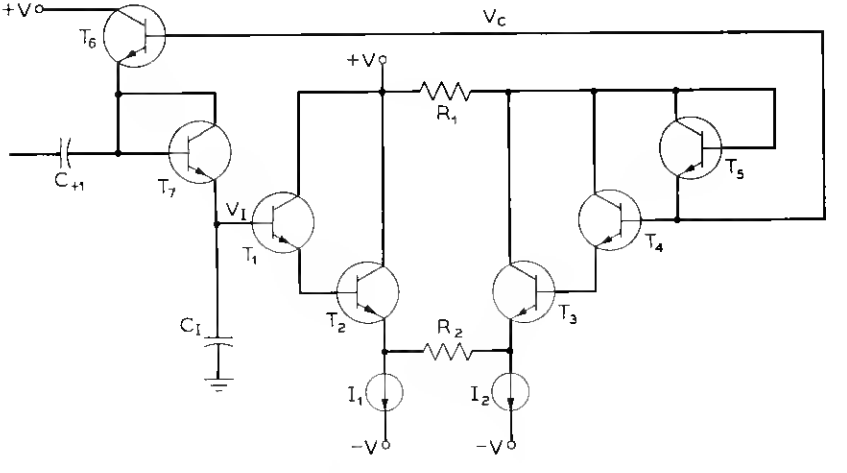

Fig. 5—Integrator step compensation circuit.

able to the current source I_2, and the excess current will be forced to flow in R_2, in this case keeping V_C more positive than V_I. Thus, the amount that C_{+1} is recharged after each voltage step becomes a function of the integrator voltage level, decreasing with increasing integrator voltage and increasing with decreasing voltage. The net effect of compensation on the +1 step size can be expressed as

$$\sigma'_{+1} = \sigma_{+1} - \Delta V_I\left(1 + \frac{R_1}{R_2}\right)^{-1}\left(\frac{C_{+1}}{C_I + C_{+1}}\right) \tag{8}$$

where σ_{+1} is the +1 step at V_I and σ'_{+1} is the +1 step at $V_I + \Delta V_I$.

Gain (loss) variation between coder and decoder is controlled by reproducing the σ_{-2} step size. This step size becomes primarily a function of the dc step control voltage, V_s, the ratio of C_{-2} to C_I, and the common base current gain of the negative step charge parceling transistor. To meet gain (loss) variation requirements, a ±1 percent tolerance is needed for both the step voltage and the capacitor ratio.

The compensation network automatically adjusts σ_{+1} in the decoder to match the σ_{+1} to σ_{-2} ratio between coder and decoder. Since a small current is derived from C_I as bias for the output buffer stage (T_1 and T_2), a drain is produced on σ_{+1}. Variations in bias current between coder and decoder cause a difference in the effective σ_{+1} step size but are counterbalanced by the compensation network. To minimize drain from C_I, a high impedance connection is made at the analog output terminal from the integrator.

3.3 *Codec Building Blocks*

Figures 6 and 7 are schematics of the comparator and the integrator circuits, respectively. A combination of a comparator and an integrator are required by the coder; only an integrator is required by the decoder. Figure 8 is the block diagram of a complete codec. Thus, a codec is implemented from 61 transistors and diodes, 54 resistors, and 6 capacitors. Transistors, diodes, and resistors are fabricated by IC techniques, the capacitors by thin-film techniques.

The comparator stage (Fig. 6) compares an analog input with an integrator output signal. Their difference is amplified by approximately 200 and is passed to a latching circuit (T_8, T_9, T_{12}). The latch holds the state of the comparator output for the duration of the clock pulse and allows conversion of the output to a single bit digital code by the clocked output gate (T_{10}, T_{11}). To avoid a race condition CLOCK1 input is made to overlap the pulse from CLOCK2 input.

The integrator network (Fig. 7) converts the clock and digital inputs

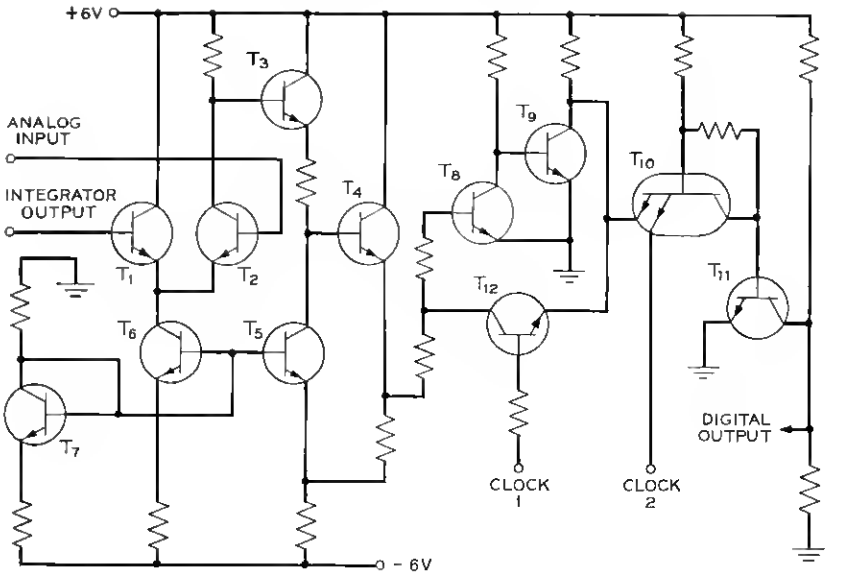

Fig. 6—ΔM comparator.

at the integrator into controlled amplitude voltage steps by first amplifying the input pulses (T_2) and then generating a voltage step (T_3, T_4) to the charge parceling circuit. The step is controlled by a voltage control (V_s = 1 volt) plus two temperature compensating diodes (T_5, T_6). The charge parceling circuit uses 33-pF and 69-pF capacitors for the +1 and −2 steps and a 2690-pF capacitor for the integrator. This allows approximately a 12-millivolt integrator step voltage. Note that the ratio of the charge parceling capacitors represents only a portion of the integrator step imbalance. The effective size of the positive step is decreased by output stage biasing requirements and by the effect of parasitic capacitances in the charge parceling network. The compensation network is designed to provide approximately 2 percent of step size compensation per volt change in the integrator output level.

IV. CODEC OPERATION

Tests were performed on codecs fabricated from discrete beam-lead resistors and transistors on ceramic substrates. Figure 9 shows a photograph of the codec ceramic. The ceramic contains the comparator and the two integrators needed for a complete codec. Discrete capacitors

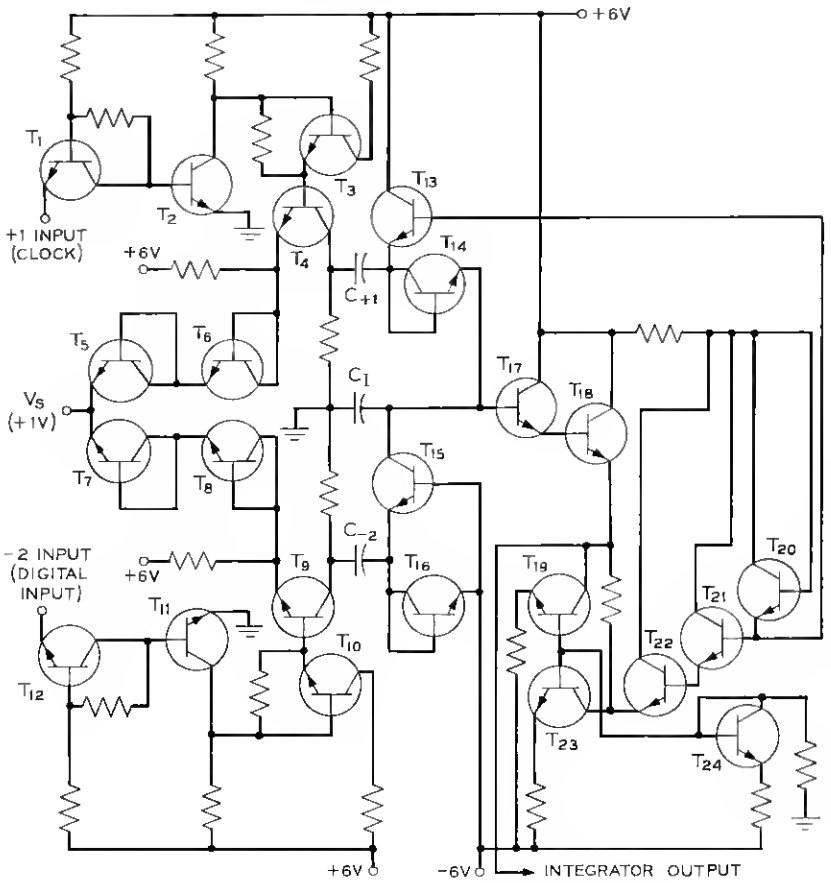

Fig. 7—ΔM integrator.

were used for the charge parceling circuit and were externally mounted to the model.

Measurements were made with a 1.544-MHz sampling frequency and a 12-millivolt integrator step size. Integrator imbalance was set at $\vartheta \approx 0.10$. Figure 10 shows typical signal-to-noise characteristics of the codec for a 3200-Hz input signal. Similar characteristics are observed for other input frequencies. Signal-to-noise ratio is well above transmission objectives. Quiescent quantizing noise is measured at less than 12 dBrnC.

Dips in the signal-to-noise curve are caused by the sawtooth error

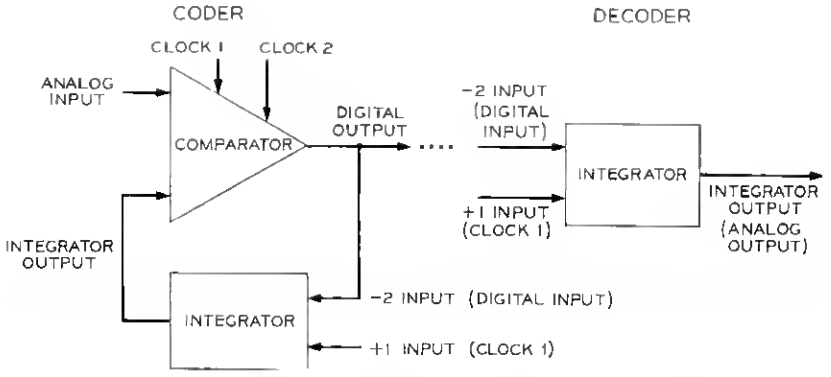

Fig. 8—Interconnecting ΔM comparator and integrator blocks to form a codec.

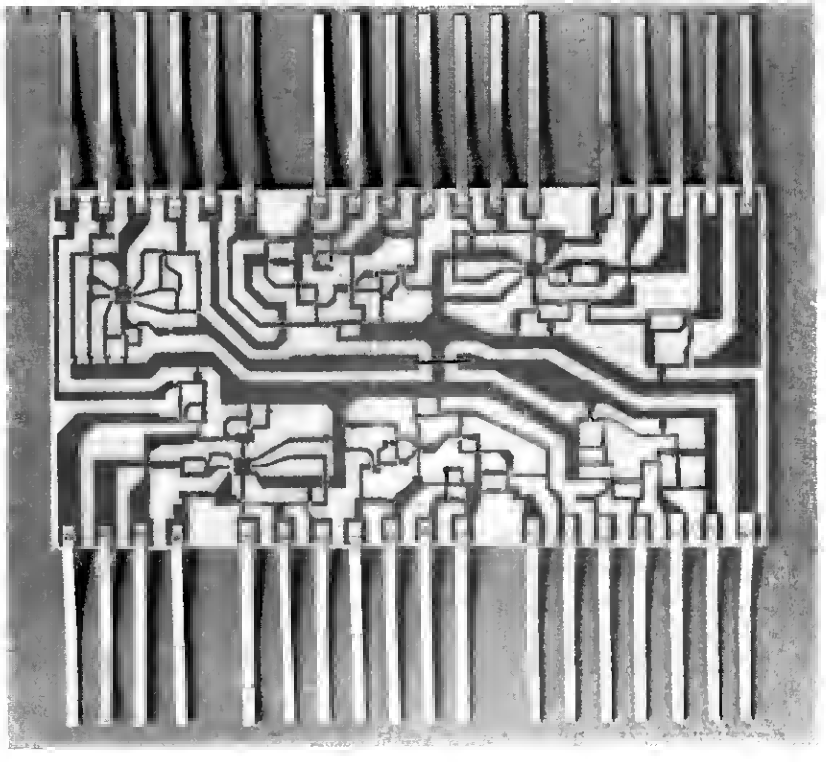

Fig. 9—Discrete beam-lead resistor and transistor model of ΔM codec.

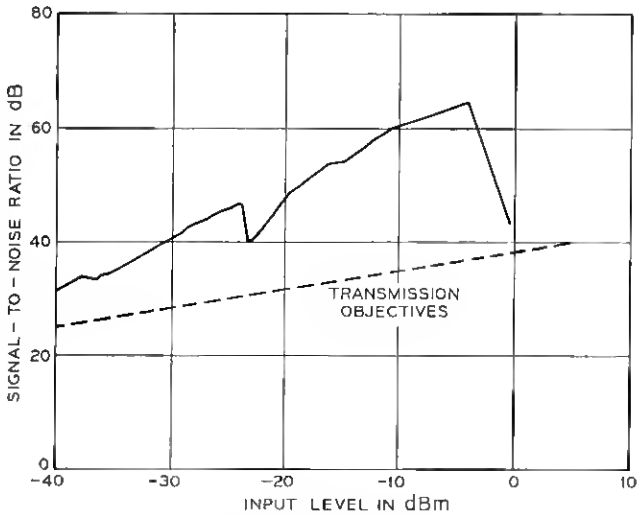

Fig. 10—Measured ΔM signal-to-quantizing noise ratio for a 3200-Hz input signal, f_s = 1.544 MHz, quiescent quantizing noise = 12 dBrnC.

waves generated hy the integrator step imhalance.[9] The largest dip in the curve (Fig. 10) occurs when the input signal slope and the fundamental sawtooth slope are approximately the same magnitude. The input signal will reduce the effective slope (and therefore increase the length) of the fundamental sawtooth; and as the sawtooth frequency is reduced to voicehand frequencies, additional noise hegins to appear in the voicehand. A worst-case condition is encountered when the resulting fundamental sawtooth error wave has heen reduced to the midhand frequency of the voice signals. For the 3200-Hz input signal this corresponds to approximately a −23-dBm (900-Ω) input signal. Additional smaller dips in the signal-to-noise curve are caused when higher order sawtooth waves are forced into voicehand; however, their effect is not significant. Thus, signal-to-noise prohlems are avoided provided that the integrators contain a sufficiently high unhalance to keep the fundamental sawtooth frequency from the voicehand until high signal levels are coded.

A numher of codecs have heen fahricated and tested using discrete heam-lead devices. All have shown similar signal-to-noise characteristics. Gain (loss) variation has heen maintained within ±0.2 dB. Power dissipation is approximately 250 milliwatts per codec.

Design of an integrated version of the codec has also heen completed

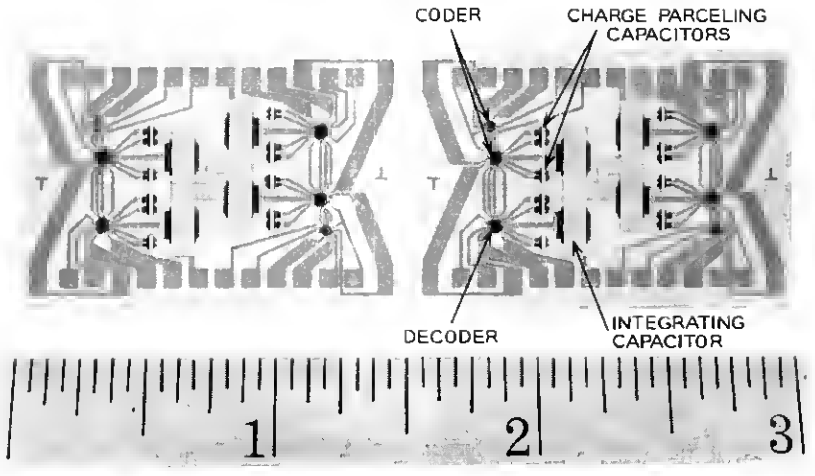

Fig. 11—Four integrated ΔM codecs using thin-film charge parceling capacitors.

and preliminary tests have indicated satisfactory codec operation. The codec is fabricated from three IC chips—one comparator chip and two identical integrator chips. Figure 11 shows a ceramic substrate containing four complete codecs. Thin-film capacitors are used in the charge parceling circuits. To relieve fabrication tolerance requirements, the integrated circuit models use approximately twice the capacitor values of the discrete model.

V. CONCLUSIONS

Delta modulation techniques offer highly integrable and economical analog-to-digital conversion elements. We have described a delta modulation codec design suitable for voiceband applications where conversion economy and quality are more important than the transmission bandwidth requirements.

Techniques are utilized in the design to force a large portion of quantizing noise out of voiceband by using a controlled step imbalance in the integrator. Excellent noise characteristics are achieved. The design attempts to take advantage of integrated circuit techniques and thin-film capacitor techniques by relying on matching of device characteristics and on accurate capacitor ratio tolerances for reproducing coding characteristics. Gain (loss) variations have been maintained within

±0.2 dB using codecs fabricated from discrete beam-lead transistors and resistors.

VI. ACKNOWLEDGMENTS

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APPENDIX

Charge Parceling—Effect of Junction Capacitances on Integrator Step Size

The +1 step portion of the charge parceling circuit, including transistor junction capacitances, can be represented as shown in Fig. 12. For $\Delta V' \leqq V_{BE_1} + V_{BE_2}$, the circuit is approximated by Fig. 13. Before T_2 beings to conduct, $\Delta V'$ must increase by $V_{BE_1} + V_{BE_2}$ from its initial value. This requires a voltage swing of $\Delta V''$ at the input, where $\Delta V'' < \Delta V$. The magnitude of $\Delta V''$ is given by

$$(V_{BE_1} + V_{BE_2})(C_{TS_2} + C_{TE_1} + C_{TE_2}) = (\Delta V'' - V_{BE_1} - V_{BE_2})C_{+1}$$

or

$$\Delta V'' = (V_{BE_1} + V_{BE_2})\left(1 + \frac{C_{TS_2} + C_{TE_2} + C_{TE_1}}{C_{+1}}\right).$$

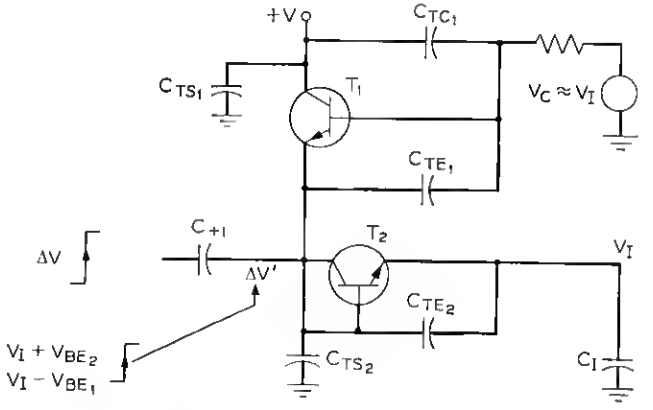

Fig. 12—+1 step portion of the charge parceling circuit.

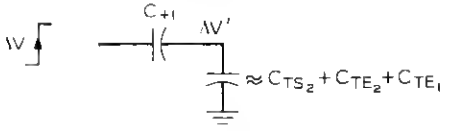

Fig. 13—Approximated circuit (+1 step) for $\Delta V' \leqq V_{BE_1} + V_{BE_2}$.

Thus, charge is dumped on C_I only for a portion of the input swing, $\Delta V - \Delta V''$. After T_2 conducts, the equivalent circuit becomes the one shown in Fig. 14, and

$$(\Delta V - \Delta V'' - \Delta V_I)C_{+1} = \Delta V_I C_I$$

or

$$\Delta V_I = (\Delta V - \Delta V'') \frac{C_{+1}}{C_I + C_{+1}},$$

and

$$\sigma_{+1} = \Delta V_I = \left[\Delta V - (V_{BE_1} + V_{BE2}) \cdot \left(1 + \frac{C_{TS_2} + C_{TE_1} + C_{TE_2}}{C_{+1}}\right)\right] \frac{C_{+1}}{C_I + C_{+1}}.$$

Note that this does not include the change in the effective +1 step size due to biasing current requirements of the output buffer stage.

A voltage step is also produced on C_I due to C_{TE_2}; however, the positive and negative portions are essentially the same and the effect is self-canceling. The −2 step portion of the charge parceling circuit is given by Fig. 15. For $\Delta V' \leqq V_{BE_1} + V_{BE_2}$, the circuit is approximated by Fig. 16.

Before T_1 conducts ΔV must change $\Delta V'$ by $V_{BE_1} + V_{BE_2}$. The

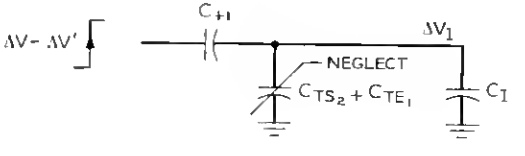

Fig. 14—Equivalent circuit for +1 step charge transfer.

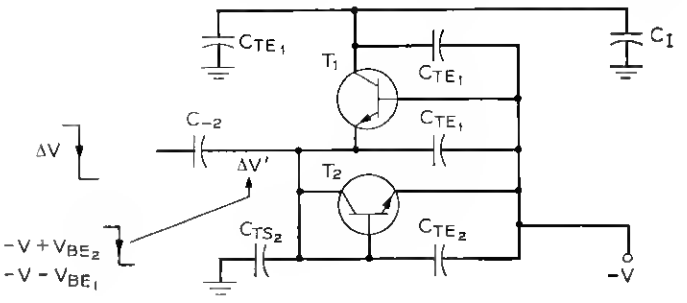

Fig. 15——2 step portion of the charge parceling circuit.

magnitude of this voltage change at input, $\Delta V''$, is given by

$$(V_{BE_1} + V_{BE_2})(C_{TS_2} + C_{TE_1} + C_{TE_2}) = (\Delta V'' - V_{BE_1} - V_{BE_2})C_{-2}$$

or

$$\Delta V'' = (V_{BE_1} + V_{BE_2})\left(1 + \frac{C_{TS_2} + C_{TE_1} + C_{TE_2}}{C_{-2}}\right).$$

Thus, charge is drained from C_I during the voltage swing $\Delta V - \Delta V''$. After T_1 conducts, the equivalent circuit is as shown in Fig. 17, and

$$\Delta V_I = (\Delta V - \Delta V'')\frac{\alpha_2 C_{-2}}{C_I + \alpha_2 C_{-2}}$$

or

$$\sigma_{-2} = \Delta V_I = \left[\Delta V - (V_{BE_1} + V_{BE_2}) \cdot\left(1 + \frac{C_{TS_2} + C_{TE_1} + C_{TE_2}}{C_{-2}}\right)\right]\frac{\alpha_2 C_{-2}}{C_I + \alpha_2 C_{-2}}.$$

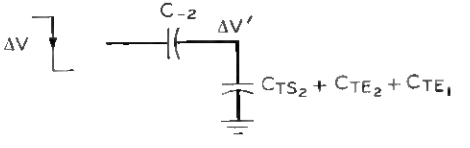

Fig. 16—Approximated circuit (−2 step) for $\Delta V' \leqq V_{BE_1} + V_{BE_2}$.

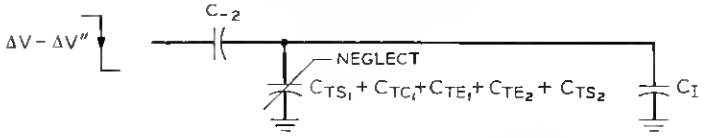

Fig. 17—Equivalent circuit for −2 step charge transfer.

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